tively constant. The emitter of either transistor **111** or **112** can be used as the output terminal for the circuit. In FIG. **7**, output **120** is coupled to the emitter of transistor **111**.

Feedback through amplifier **114** provides a constant current through the transistors. Changes in temperature cause changes in the voltage drops across transistors **111** and **112** and the difference between the voltage on the emitter of transistor **112** and the voltage at the junction of resistors **117** and **118** is used to adjust the voltage on rail **115** to maintain a substantially constant current through the transistors.

FIG. **8** is a schematic of one type of circuit suitable for use in block **85** (FIG. **5**). Voltage buffer **85** includes PMOS transistors **131** and **132** connected in series between voltage source Vdd and common. Transistors **133** and **134** are connected in series with each other and in parallel with transistor **132**. The source and gate of transistor **133** are connected together, causing the gate voltage of transistor **133** to track the voltage drop across transistor **134**. Transistors **132** and **133** are matched devices, i.e. their electrical characteristics are the same to within a small tolerance.

Transistor **131** is biased to produce a current (2i) through the transistor. This current divides between transistor **132** and transistors **133, 134**. Transistor **134** is biased to pass a current equal to i, thereby forcing a current of i through transistor **132**. Thus configured and biased, variations in the voltage on the gate of transistor **132** cause corresponding variations on the gate of transistor **133**. The gate of transistor **132** provides a very high impedance load to output **120** , thereby not affecting the measurement of temperature.

FIG. **9** is a schematic of another type of circuit that can be used for voltage buffer **85**. Buffer **140** is a differential amplifier having non-inverting input transistor **141** and inverting input transistor **142**. The gate of transistor **142** is coupled to output **145**. Transistor **147** provides a common, constant current path to ground. The gate of transistor **141** provides a very high impedance load to output **120** (FIG. **7**), thereby not affecting the measurement of temperature. Buffer **140** could also be represented schematically by the same symbol used for amplifier **114** in FIG. **7**, with the output coupled to the (−) input.

The invention thus provides an adaptive temperature control circuit in which the output signal is pulse width modulated at a high frequency. The circuit can be implemented as a single integrated circuit and can interface directly with a microprocessor for setting temperature. The circuit is easily calibrated and the voltage versus temperature curve is easily adjusted over a wide range of slopes, enabling the circuit to be used with systems of widely different response times.

Having thus described the invention, it will be apparent to those of skill in the art that various modifications can be made within the scope of the invention. For example, the low pass filter around amplifier **41** can include discrete, passive devices in a simple circuit, as illustrated, or a more complex low pass filter. For example, resistor **45** can be implemented as a circuit simulating a resistor and capacitor **46** can be replaced by a switched capacitor circuit. In either case, the feedback loop becomes programmable, which is useful in many applications. Other circuits can be substituted for the circuits illustrated in FIGS. **7** and **8**.

What is claimed as the invention is:

1. An adaptive temperature control circuit comprising:

a first circuit for producing an error signal representing the difference between a preset temperature and an actual temperature, said first circuit including a pair of PN junctions and a constant current source coupled to a first PN junction for regulating the current through a second PN junction; and

a second circuit coupled to said first circuit for producing a pulse width modulated output signal having a frequency greater than one hertz, wherein the width of the pulses is proportional to said error signal.

2. The adaptive temperature control circuit as set forth in claim **1** wherein at least said PN junctions and said second circuit are implemented on the same semiconductor die.

3. The adaptive temperature control circuit as set forth in claim **1** wherein said first circuit includes an A/D converter for providing a digital representation of temperature.

4. The adaptive temperature control circuit as set forth in claim **1** wherein said first circuit includes:

a temperature sensor producing a first signal;

a D/A converter producing a second signal indicative of a preset temperature;

a comparator having a first input coupled to said temperature sensor and a second input coupled to said D/A converter, said comparator producing said error signal.

5. The adaptive temperature control circuit as set forth in claim **4** wherein said second circuit includes:

an oscillator producing a sawtooth signal;

an amplifier having a first input coupled to said oscillator for receiving said sawtooth signal and a second input coupled to said comparator, said amplifier producing an output signal that changes state when the sawtooth signal is equal in magnitude to the error signal, thereby producing said pulse width modulated output signal.

6. The adaptive temperature control circuit as set forth in claim **5** wherein said second circuit further includes a control circuit coupled to said amplifier for limiting the pulse width of said pulse width modulated output signal.

7. The adaptive temperature control circuit as set forth in claim **1** wherein said first circuit includes:

a voltage buffer having an input coupled to said junction and an output, said voltage buffer producing a signal indicative of the temperature of said second PN junction on said output;

a source of reference voltage;

a first resistor and a second resistor coupled in series between said source and common and having a junction therebetween;

an operational amplifier having a first input coupled to the output of said voltage buffer and a second input coupled to said junction;

a third resistor coupled between an output of said operational amplifier and said first input;

wherein said second resistor is variable and controls an offset voltage and said third resistor is variable and controls the gain of said operational amplifier.

8. Apparatus for producing an electrical error signal representing the difference between a preset temperature and an actual temperature, said apparatus comprising:

at least one PN junction;

a voltage buffer having an input coupled to said junction and an output, said buffer circuit producing a signal indicative of the temperature of said PN junction on said output;

a source of reference voltage;

a first resistor and a second resistor coupled in series between said source and common and having a junction therebetween;

an operational amplifier having a first input coupled to the output of said voltage buffer and a second input coupled to said junction;

a third resistor coupled between an output of said operational amplifier and said first input;

wherein said second resistor is variable and controls an offset voltage and said third resistor is variable and controls the gain of said operational amplifier.

9. The apparatus as set forth in claim **8**, wherein said voltage buffer includes:

a first transistor having an input terminal coupled to said junction, a second transistor coupled to said operational amplifier, and a third transistor, wherein the first transistor and the second transistor are coupled in parallel with each other and in series with the third transistor;

said third transistor limiting the sum of the currents through the first transistor and the second transistor and causing changes in the input voltage to the first transistor to be reflected as changes in the voltage drop across the second transistor, whereby the voltage on said junction is isolated from said operational amplifier.

* * * * *

CLAIM 10. A temperature responsive control circuit comprising:

a first circuit for producing a first signal representing the difference between a predetermined temperature and an actual temperature, said first circuit comprising a bandgap; and

a second circuit coupled to said first circuit and responsive to said first signal to produce a pulse width modulated output signal, wherein the width of the pulses of said pulse width modulated output signal has a predetermined relationship to said first signal.

CLAIM 11. A temperature responsive control circuit in accordance with claim 10, comprising:

a semiconductor die having at least said first and said second circuits formed thereon.

CLAIM 12. A temperature responsive control circuit in accordance with claim 10, wherein

said first circuit generates said first signal as a digital signal.

CLAIM 13. A temperature responsive control circuit in accordance with claim 10, wherein:

said first circuit comprises a comparator for comparing a signal from said bandgap and a signal indicative of a predetermined temperature to generate said first signal.

CLAIM 14. A temperature responsive control circuit in accordance with claim 13, wherein:

said signal indicative of a predetermined temperature is generated by a digital signal source.

CLAIM 15. A temperature responsive control circuit in accordance with claim 14, wherein:

said digital signal source is a microprocessor.

CLAIM 16. A temperature responsive control circuit in accordance with claim 14, wherein:

said first circuit comprises a digital to analog converter coupling said digital signal source to said comparator.

CLAIM 17. A temperature responsive control circuit in accordance with claim 13, wherein

said second circuit comprises a sawtooth signal generator and a circuit responsive to said sawtooth signal generator and to said first signal to produce said pulse width modulated output signal.

CLAIM 18. A temperature responsive control circuit in accordance with claim 17, wherein

said second circuit comprises a control circuit coupled to said circuit responsive to said sawtooth signal generator for limiting the pulse width of said pulse width modulated output signal.

CLAIM 19. A temperature control circuit as set forth in claim 10, wherein:

said first circuit comprises: an operational amplifier coupled to said bandgap; first and second series connected resistors coupled to said operational amplifier, said second resistor cooperating with said operational amplifier such that the selection of the value of said second resistor controls the offset voltage of said operational amplifier; and a third resistor coupled to said operational amplifier, the resistance value of said third resistor being selected to control the gain of said operational amplifier.

CLAIM 20. A temperature sensor, comprising:

a bandgap comprising at least one PN junction subject to temperature variations for generating a temperature dependent voltage;

an operational amplifier having a first input coupled to said PN junction and providing an output signal having a magnitude representative of the temperature of said PN junction, said output signal magnitude having a substantially linear relationship to the temperature of said PN junction;

a first resistance coupled to said operational amplifier, the value of said first resistance being selected to determine an offset voltage of said operational amplifier; and

a second resistance coupled to said operational amplifier, the value of said second resistance being selected to adjust the gain of said operational amplifier.

CLAIM 21. A temperature sensor in accordance with claim 20, comprising:

an integrated circuit having at least said PN junction, said operational amplifier, said first resistance and said second resistance formed thereon.

CLAIM 22. A temperature sensor in accordance with claim 20, comprising:

an analog-to-digital circuit coupled to operational amplifier for providing a digital output signal representative of the temperature of said PN junction.

CLAIM 23. A temperature sensor, comprising:

at least one PN junction responsive to temperature variations for generating a temperature dependent voltage;

an operational amplifier having a first input coupled to said PN junction and providing an output signal having a magnitude representative of the temperature of said PN junction, said output signal magnitude having a substantially linear relationship to the temperature of said PN junction;

a first resistance coupled to said operational amplifier; and

a second resistance coupled to said operational amplifier

said bandgap, said operational amplifier, and said first and second resistances cooperatively operating such that the output voltage of said operational amplifier varies with respect to said PN junction temperature in accordance with a substantially linear characteristic curve: and

whereby the selection of the resistance value of said first resistance determines the offset of said curve and the selection of the resistance value of said second resistance value determines the slope of said curve.

CLAIM 24. A temperature sensor in accordance with claim 23, comprising:

an integrated circuit having said PN junction, said operational amplifier, said first resistance and said second resistance formed thereon.

CLAIM 25. A temperature sensor in accordance with claim 24, wherein:

said integrated circuit comprises an analog to digital converter coupled to the output of said operational amplifier.

CLAIM 26. Apparatus for monitoring temperature, comprising:

an integrated circuit comprising:

at least one PN junction responsive to temperature variations for generating a temperature dependent voltage;

an operational amplifier having a first input coupled to said PN junction and providing an output signal having a magnitude representative of the temperature of said PN junction, said output signal having a substantially linear characteristic curve relationship to the temperature of said PN junction;

a first resistance coupled to said operational amplifier; and

a second resistance coupled to said operational amplifier

said at least one PN junction, said operational amplifier, and said first and second resistances cooperatively operating such that the output voltage of said operational amplifier varies with respect to said PN junction temperature in accordance with a substantially linear characteristic curve; and

whereby the selection of the value of said first resistance determines the offset of said curve and the selection of the value of said second resistance value determines the slope of said curve.

CLAIM 27. Apparatus in accordance with claim 26, wherein:

said integrated circuit comprises an analog-to-digital coupled to said operational amplifier for providing digital output signals representative of said temperature of said PN junction.

CLAIM 28. Apparatus in accordance with claim 26, comprising:

a second PN junction coupled to said PN junction.

CLAIM 29. A method of manufacturing an integrated circuit comprising an adaptive temperature control circuit thereon, said method comprising the steps of:

fabricating said integrated circuit comprising said adaptive temperature control circuit, said adaptive temperature control circuit comprising a first circuit for producing a first signal representing the difference between a predetermined temperature and an actual temperature; and a second circuit coupled to said first circuit and responsive to said first signal to produce a pulse width modulated output signal, wherein the width of the pulses of said pulse width modulated output signal has a predetermined relationship to said first signal;

providing at least first and second selectable resistances on said integrated circuit;

determining two points on an output response curve for said adaptive temperature control circuit;

selecting the values of said first and said second resistances to calibrate said response curve to desired response.

CLAIM 30. A method in accordance with claim 29, comprising:

fabricating said first circuit to comprise a bandgap.

CLAIM 31. A method in accordance with claim 29, comprising:

selecting the value of said first resistance to obtain vertical translation without rotation of said output responsive curve.

CLAIM 32. A method in accordance with claim 31, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 33. A method in accordance with claim 29, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 34. A method in accordance with claim 30, comprising:

selecting the value of said first resistance to obtain vertical translation without rotation of said output responsive curve.

CLAIM 35. A method in accordance with claim 34, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 36. A method in accordance with claim 30, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 37. A method of manufacturing an integrated circuit comprising an adaptive temperature control circuit thereon, said method comprising the steps of:

fabricating said integrated circuit comprising said adaptive temperature control circuit, said adaptive temperature control circuit comprising a first circuit for producing a first signal representing the difference between a predetermined temperature and an actual temperature; and a second circuit coupled to said first circuit and responsive to said first signal to produce a pulse width modulated output signal, wherein the width of the pulses of said pulse width modulated output signal has a predetermined relationship to said first signal;

providing a first resistance on said integrated circuit;

measuring the output response of said adaptive temperature control circuit to

determine a first point on an output response curve for said adaptive temperature control circuit;

selecting the value of said first resistance to calibrate a first characteristic of said response curve to a desired characteristic.

CLAIM 38. A method in accordance with claim 37, comprising:

providing a second resistance on said integrated circuit;

measuring the output response of said adaptive temperature control circuit to determine a second point on said output response curve.

selecting the value of said second resistance to calibrate a second characteristic of said response curve to a second desired characteristic.

CLAIM 39. A method in accordance with claim 37, comprising:

fabricating said first circuit to comprise a bandgap.

CLAIM 40. A method in accordance with claim 37, comprising:

selecting the value of said first resistance to obtain vertical translation without rotation of said output responsive curve.

CLAIM 41. A method in accordance with claim 38, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 42. A method in accordance with claim 41, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 43. A method of manufacturing an integrated circuit comprising a temperature sensing circuit thereon, said method comprising the steps of:

fabricating said temperature sensing circuit comprising a first circuit for producing a first signal representing a sensed temperature;

providing first and second resistances on said integrated circuit;

determining two points on an output response curve for said adaptive temperature control circuit;

selecting the values of said first and said second resistances to calibrate said response curve to desired response.

CLAIM 44. A method in accordance with claim 43, comprising:

fabricating said first circuit to comprise a bandgap.

CLAIM 45 A method in accordance with claim 43, comprising:

selecting the value of said first resistance to obtain vertical translation without rotation of said output responsive curve.

CLAIM 46. A method in accordance with claim 45, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 47. A method in accordance with claim 43, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 48. A method in accordance with claim 44, comprising:

selecting the value of said first resistance to obtain vertical translation without rotation of said output responsive curve.

CLAIM 49. A method in accordance with claim 48, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 50. A method in accordance with claim 44, comprising:

selecting the value of said second resistance to obtain rotation without translation of said output responsive curve.

CLAIM 51 A circuit for controlling utilization apparatus in response to a sensed environmental parameter, said circuit comprising:

a semiconductor die comprising:

a temperature responsive circuit operable to generate a temperature dependent output signal;

a programmable temperature control circuit for generating reference signals representative of a desired temperature level;

a comparator coupled to said temperature responsive circuit and to said programmable temperature control circuit for generating an error signal representative of the difference between said desired temperature level and the temperature represented by said temperature dependent output signal; and

a driver circuit coupled to said comparator for providing utilization apparatus control signals.

CLAIM 52. A circuit in accordance with claim 51, wherein:

said utilization apparatus control signals are pulse width modulated signals.

CLAIM 53. A circuit in accordance with claim 51, wherein:

said semiconductor die comprises:

a pulse width modulator disposed between said comparator and said driver circuit.

CLAIM 54. A circuit in accordance with claim 51, wherein:

said temperature responsive circuit comprises a bandgap.

CLAIM 55. A circuit in accordance with claim 51, wherein:

said programmable temperature control circuit comprises circuitry responsive to digital signals.

CLAIM 56. A circuit in accordance with claim 51, wherein:

said semiconductor die comprises a first selectable paramater value for calibrating a first characteristic of said temperature responsive circuit.

CLAIM 57. A circuit in accordance with claim 56, wherein:

said semiconductor die comprises a second selectable parameter value for calibrating a second characteristic of said temperature responsive circuit.

CLAIM 58. An adaptive temperature control circuit comprising:

a first circuit comprising a pair of PN junctions, said first circuit producing an error signal representing the difference between a preset temperature and the actual temperature of said PN junctions, said error signal having a predetermined relationship to said difference; and

a second circuit coupled to said first circuit for producing a pulse width modulated output signal, wherein the width of the pulses of said pulse width modulated output signal has a second predetermined relationship to said error signal.

CLAIM 59. An adaptive temperature control circuit in accordance with claim 58, wherein

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 60. An adaptive temperature control circuit in accordance with claim 58, wherein:

said first circuit comprises an A/D converter coupled to said first circuit and responsive thereto to provide a digital representation of temperature.

CLAIM 61. An adaptive temperature control circuit in accordance with claim 60, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 62. An adaptive temperature control circuit in accordance with claim 58, wherein said first circuit comprises:

circuitry coupled to said PN junctions to produce a first signal;

a D/A converter producing a second signal indicative of a preset temperature;

a comparator having a first input coupled to said circuitry and a second input coupled to said D/A converter, said comparator producing said error signal.

CLAIM 63. An adaptive temperature control circuit in accordance with claim 62, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 64. An adaptive temperature control circuit as set forth in claim 62, wherein:

said second circuit comprises an oscillator and second circuitry coupled to said oscillator and to said error signal to produce said pulse width modulated output signal.

CLAIM 65. An adaptive temperature control circuit in accordance with claim 64, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 66. An adaptive temperature control circuit in accordance with claim 64, wherein:

said oscillator generates a sawtooth signal;

said second circuitry comprises an amplifier having a first input coupled to said oscillator for receiving said sawtooth signal and a second input coupled to said comparator, said amplifier producing an output signal that changes state when the sawtooth signal is equal in magnitude to the error signal, thereby producing said pulse width modulated output signal; and

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 67. An adaptive temperature control circuit in accordance with claim 58, wherein:

said second circuit comprises a control circuit to limit the pulse width of said pulse width modulated output signal.

CLAIM 68. An adaptive temperature control circuit in accordance with claim 58, wherein:

an operational amplifier coupled to said pair of PN junctions;

a first resistor coupled to said operational amplifier and having a value selected to control an offset voltage of said operational amplifier; and

a second resistor coupled to said operational amplifier and having a value selected to control the gain of said operational amplifier.

CLAIM 69. An adaptive temperature control circuit in accordance with claim 68, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 70. An adaptive temperature control circuit in accordance with claim 58, wherein:

said preset temperature is received by said first circuit as a digital representation of said preset temperature.

CLAIM 71. An adaptive temperature control circuit in accordance with claim 70, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 72. An adaptive temperature control circuit in accordance with claim 70, wherein:

second circuit is responsive to said error signal such that the widths of pulses of said pulse width modulated signal are determined by the sign and magnitude of the error indicated by said error signal.

CLAIM 73. An adaptive temperature control circuit in accordance with claim 72, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 74. An adaptive temperature control circuit in accordance with claim 58, wherein:

second circuit is responsive to said error signal such that the widths of pulses of said pulse width modulated signal are determined by the sign and magnitude of the error indicated by said error signal.

CLAIM 75. An adaptive temperature control circuit in accordance with claim 74, wherein:

said first circuit and said second circuit are implemented on the same semiconductor die.

CLAIM 76. An adaptive temperature control circuit, comprising:

an integrated circuit comprising:

a first circuit for generating an error signal in response to a digital signal input corresponding to a preset temperature and to a signal generated in response to the temperature of a PN junction; and

a second circuit responsive to said error signal to generate a pulse width modulated signal.

CLAIM 77. An adaptive temperature control circuit in accordance with claim 701, wherein:

_____ said first circuit comprises circuitry for generating a digital signal output indicative of said PN junction temperature.

CLAIM 78. An adaptive temperature control circuit in accordance with claim 70, wherein:

_____ said first circuit comprises at least one first component selectable to determine a first calibration temperature characteristic of said first circuit.

CLAIM 79. An adaptive temperature control circuit in accordance with claim 72, wherein:

_____ said first circuit comprises at least one second component selectable to determine a second calibration temperature characteristic of said first circuit.